MERI College of Engineering & Technology
(MERI-CET)

Session: 2020-2021
Department: CSE
Subject code: CSE-401-F

Course- CSE
Semester: 7th
Faculty Name : Ms. PREETI

Lesson plan

Name if the faculty : Ms.PREETI

Discipline : Computer Science Engineering

Semester : 7th

Subject : **ADVANCED COMPUTER ARCHITECTURE**

Lesson Plan Duration : 14 weeks (From August, 2020 to November 2020)

Work Load (Lecture/ Practical) per week (in hours): Lecture-03.

Week	Theory	
	Lecture day	Topic(Including assignment/test)
1st	1st	**Architecture And Machines,** Introduction, Some definition and terms
	2nd	interpretation and microprogramming
	3rd	The instruction set, , Basic data types
2nd	1st	Instructions, Addressing and Memory
	2nd	Virtual to real mapping
	3rd	Basic Instruction Timing
3rd	1st	**Time, Area And Instruction Sets:**Time, cost-area
	2nd	technology state of the Art
	3rd	The Economics of a processor project: A study, Instruction sets, Matrix
4th	1st	Professor Evaluation
	2nd	Revision of first unit with test
	3rd	**Cache Memory Notion:**
	4th	Basic Notion

MERI College of Engineering & Technology (MERI-CET)

Session: 2020-2021
Department: CSE
Subject code: CSE-401-F

Course- CSE
Semester: 7th
Faculty Name : Ms. PREETI

5th	1st	Widrow-Hoff learning rule
	2nd	Cache Organization,
	3rd	Cache Data, adjusting the data for cache organization,
6th	1st	write policies.
	2nd	strategies for line replacement at miss time
	3rd	Cache Environment, other types of Cache.
7th	1st	Split I and D-Caches, on chip caches
	2nd	Two level Caches
	3rd	write assembly Cache, Cache references per instruction
8th	1st	technology dependent Cache considerations
	2nd	virtual to real translation
	3rd	overlapping the Tcycle in V-R Translation. studies. Design summary
9th	1st	Revision of 2nd unit with test
	2nd	**Memory System Design:**
	3rd	The physical memory, processor memory modeling using queuing theory
10th	1st	open, closed and mixed-queue models,
	2nd	waiting time, performance
	3rd	and buffer size, review and selection of queuing models,
11th	1st	processors with cache.
	2nd	Revision of 3rd unit with test
	3rd	**Concurrent Processors:** Vector Processors
12th	1st	Training & Examples
	2nd	Vector Memory,
	3rd	Multiple Issue Machines, Comparing vector and Multiple Issue processors.
13th	1st	**Shared Memory Multiprocessors:** Basic issues
	2nd	partitioning

	3rd	synchronization and coherency, Type of shared Memory multiprocessors,
14th	1st	Memory Coherence in shared Memory Multiprocessors.
	2nd	Revision of 4th unit with test
	3rd	Overall Revision